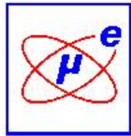


Micro-RDC

Microelectronics Research Development Corporation

THE AEROSPACE CORPORATION

# Multiple Bit Upsets and Error Mitigation in Ultra Deep Submicron SRAMs

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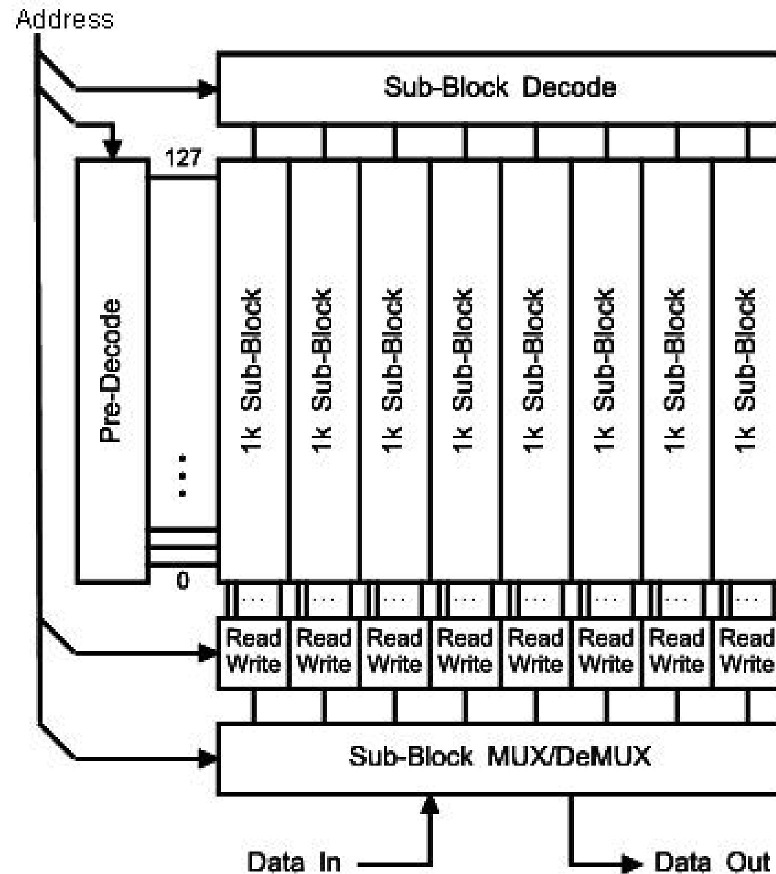
# Outline

- SRAM test coupon
- Test and analysis procedures
- SRAM scrubbing investigations
- Conclusions

# SRAM Test Structure Architecture

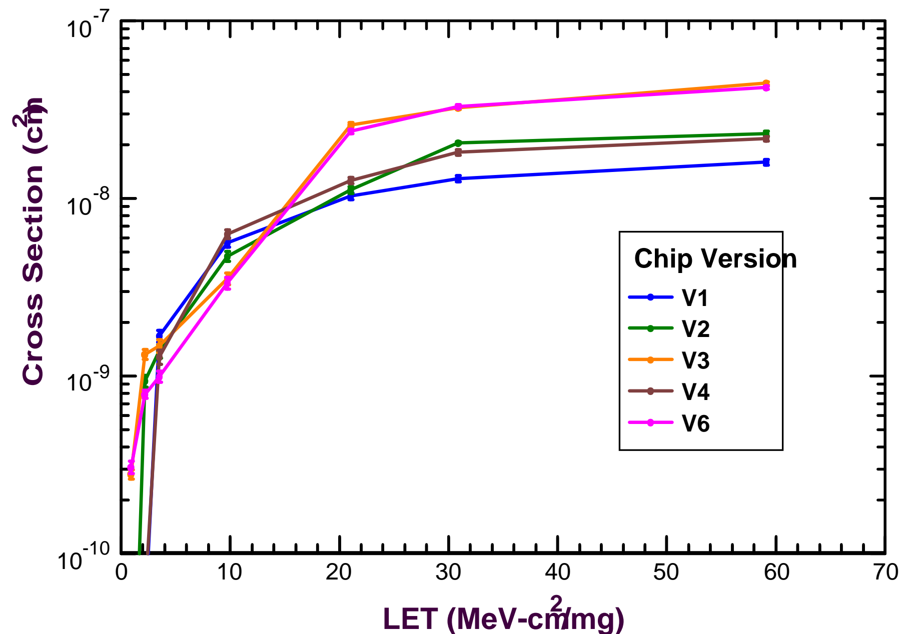



8kx1 Memory Block

- 8k x 8 EDAC protected stand alone memory
  - 12-8kx1 bit blocks
  - 8 blocks data
  - 4 blocks check bits
  - Addressed as 8k x 8 architecture
    - 13 address bits
    - 8 data bits in, 12 data bits out
  - Block separation 100 ~m
- Five variations designed and fabricated in a bulk 90-nm CMOS process

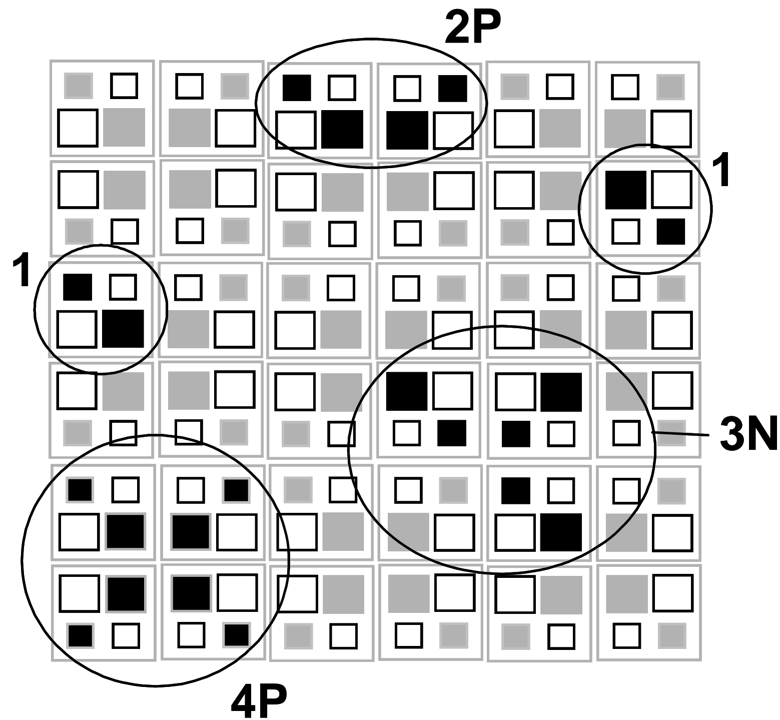
# SEU Testing

## Traditional SEU Results




- **New Methodology**
  - Normally incident heavy ions
  - Physical checkerboard
  - EDAC off
    - Memory polled and scrubbed every 5.6 ms
  - At each poll, record:
    - Error address
    - Data written to memory
    - Data read from memory
    - Time stamp when error occurred
  - Post process log file
    - Map errors to physical layout
    - Identify multi-cell upsets
    - Categorize type of upset

# Extended SEU Analysis Approach

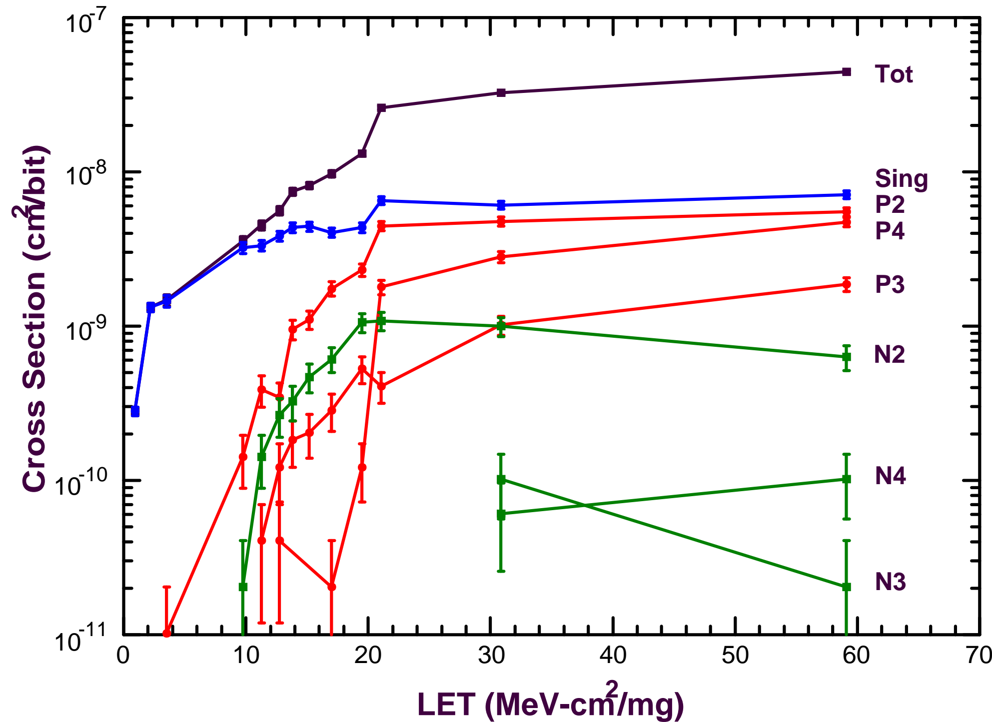



Reverse-biased drain-to-well in bit cell (sensitive to SEU)

Transistor pair struck corresponding to SEU error

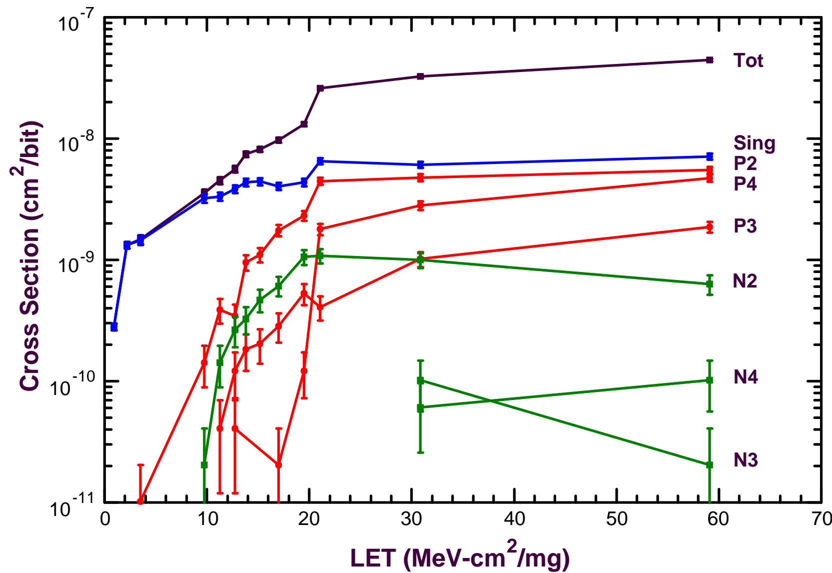
Example graphical representation of SEU testing results

# New Results Show Errors Dominated by MCUs



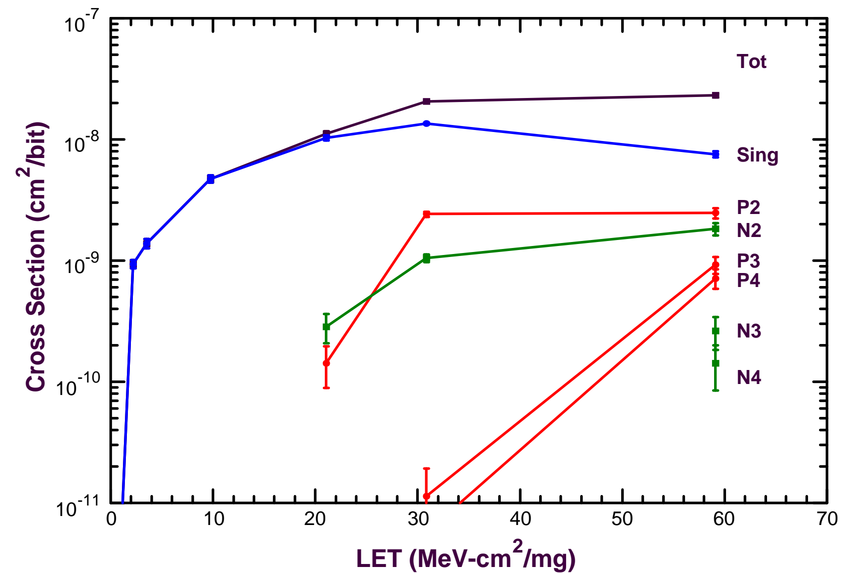

- Single-cell upsets: 18%
- Multi-cell upsets: 82%
- All MCUs caused by single particle strikes
  - Probability of 2 bits upsetting from 2 different particles strikes ~ $2x10^{-6}$

# PMOS SEU Sensitivity




- SRAM with increased critical node spacing shows reduced error rates
  - Consistent with lack of observed MCUs in older techologies

- PMOS nodes the most sensitive in dense SRAM
  - Consistent with turn-on of PNP parasitic bipolar devices within a common n-well



# Scrubbing Rate Relation

- For
  - $R_b$ as the SEU errors/bit-day error rate (the inherent SRAM error rate with no EDAC and no scrubbing,
  - $R_{be}$ as the desired effective errors/bit-day error rate (the effective error rate achievable after EDAC and scrubbing), and
  - N as the number of memory words, L as the data word length, and P the number of parity bits needed for EDAC, then

$$R_{mbu} = \tfrac{1}{2} \cdot T_{scrub} \cdot N \cdot (L+P)^2 \cdot R_b^2$$

$$R_{mbu} = N \cdot L \cdot R_{be}$$

- Which means, the scrubbing rate $T_{scrub}$ necessary to achieve a given error rate $R_b$ is given by:

$$T_{scrub} = 2 \cdot \frac{R_{be}}{R_b^2} \cdot \frac{L}{(L+P)^2}$$

# Experimental Verification

- Scrubbing fundamental equations experimentally verified
  - Vary beam flux and measure at two different SEU rates
  - Vary time between scrubs and compare normalized results to expected

**From:**

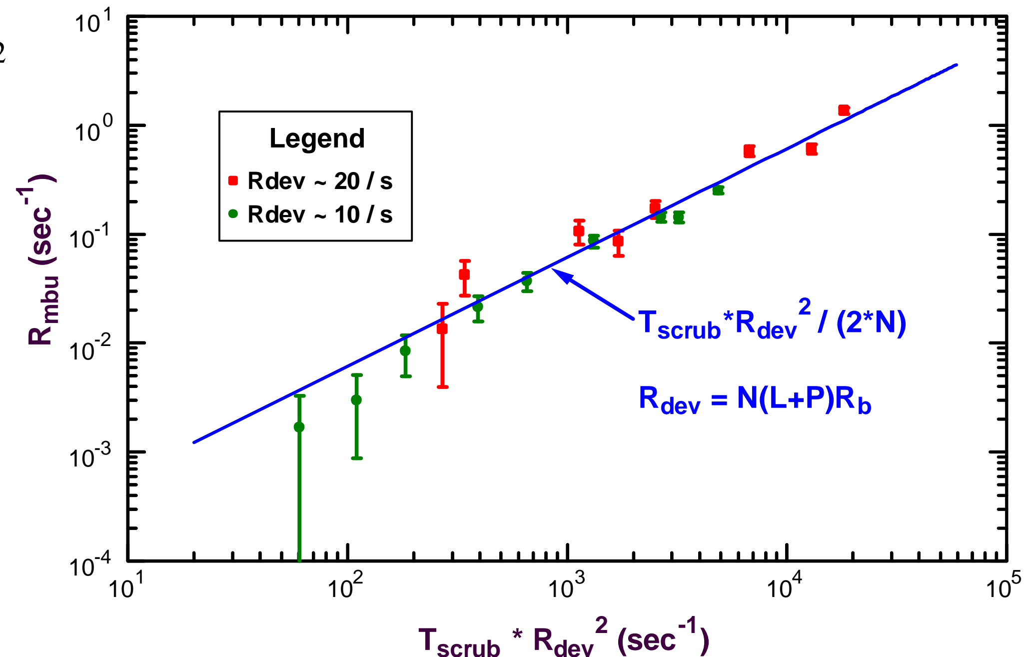
$$R_{mbu} = \frac{1}{2} \cdot T_{scrub} \cdot N \cdot (L+P)^2 \cdot R_b^2$$

**With:**

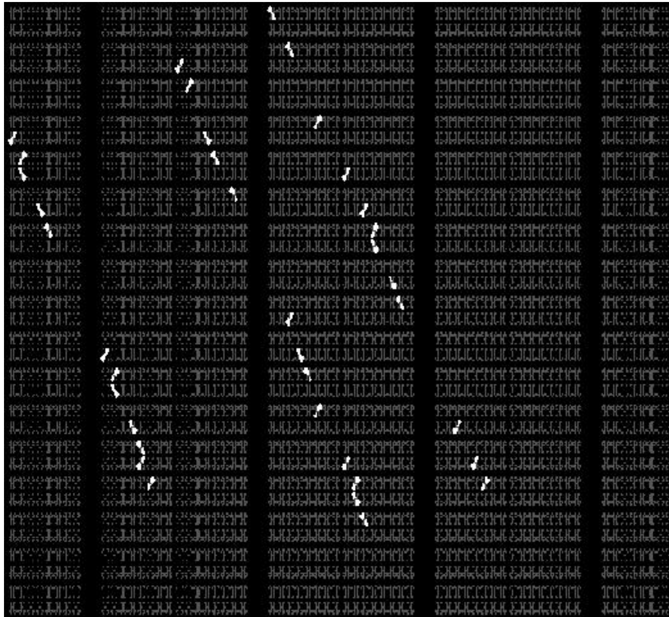
$$R_{dev} = N \cdot (L+P) \cdot R_b$$

**Predicted error rate:**

$$R_{mbu} = T_{scrub} \cdot R_{dev}^2 / (2 \cdot N)$$

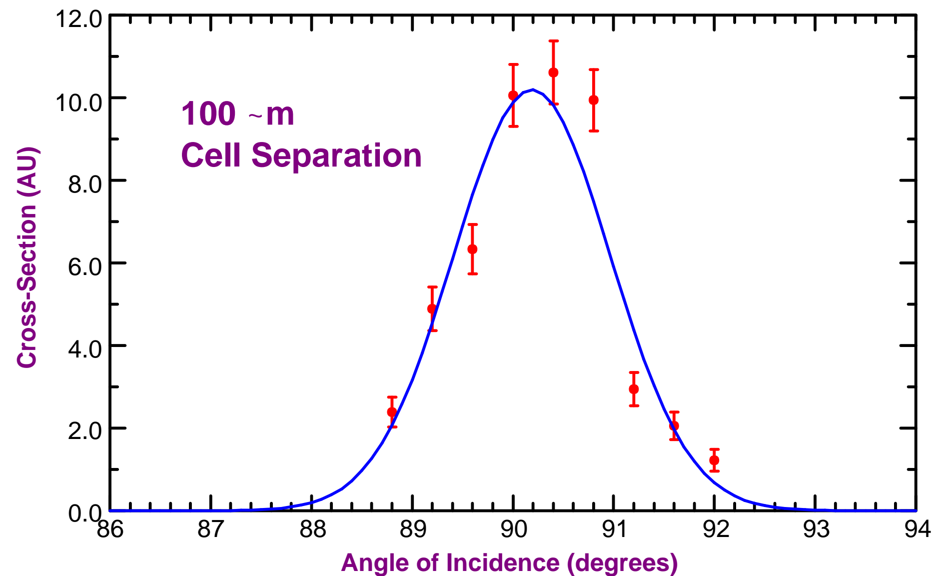


# MCUs in Realistic Heavy-Ion Environment



- 90° incident heavy ions
- Ne ion in the LBL 16A MeV cocktail
- Range ~240 µm

- Step angle of incidence
- Measure separation of each MCU
- Least-squares fit provides MCU integration over solid angle
- Width ***NOT*** necessarily related to angle subtended between nodes

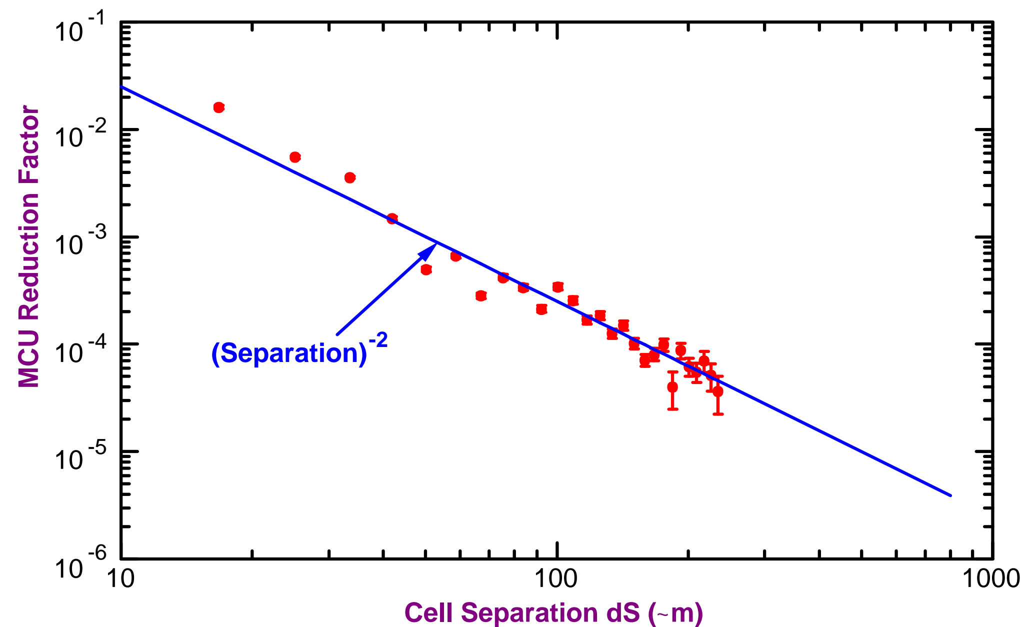


# Efficacy of Scrubbing

- Compare the MCU integrated error rates to the $2f$ • SCU rate
  - Crème predicts SEU rates ~ $10^{-8}$ errors/bit-day
  - $10^4$ MBU rate reduction at ~100 µm separation
  - Pointless to scrub to better than $10^{-12}$ errors/bit-day

- Given a 32 Mbit SRAM
  - N = 1 M Words
  - L = 32 bits
  - P = 6 bits

- Desired $T_{scrub}$
  - 443 days (in Geo-synchronous orbit)
  - 2.8 hours (for worst case proton orbit)



# Conclusions

- Nano-Scale CMOS SRAMs ➔ Show an increased MCU sensitivity
  - Ionization track can directly intercept multiple bit cells
  - Diffusion charge easily shared between multiple bit cells
  - Parasitic bipolar effects enhance upsets of multiple bit cells sharing a common n-well

- Simple EDAC with scrubbing can be effective for error mitigation
  - Bit cell separation within a word should be > 100 µm
  - Satisfied by a block based architecture of 6T cell designs
  - Resulting scrubbing rates acceptable for even large SRAMs